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EXAMINER	
GEBREMARIAM, SAMUEL A	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,526	POPHRISTIC ET AL.	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-76* is/are pending in the application.

4a) Of the above claim(s) *37-70 and 74-76* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36 and 71-73* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/25/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of group I, claims 1-36 and 71-73 drawn to a method of making a semiconductor device is acknowledged.

Specification

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

3. Claim 29 recites the limitation "first metal" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 4 and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 4, the claimed limitation of "diffusing dopants from said sub-layer of doped nitride semiconductor into said sub-layer of undoped nitride semiconductor" is unclear as to what happens to the doped after the end of the diffusion process.

Regarding claim 30, the structural relationship between said doped layer the claimed device is not clear.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

7. Claims 1-2 and 4-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al., Pub. No. US 2003/0010993 in view of Parikh et al, WO 03/026021.

Regarding claim 1, Nakamura teaches (fig. 1) a method of forming a semiconductor layer structure, the method comprising: forming a modulation doped layer (4) atop at least a portion of another layer (3) by forming at least one sub-layer of doped nitride semiconductor (refer to paragraph [0054]) and at least one sub-layer undoped nitride semiconductor (refer to paragraph [0054]) atop the at least portion of the another layer (3).

Nakamura does not explicitly state that the modulation-doped layer has a doping concentration of at most 2E16cm $^{-3}$.

Parikh teaches n-doped GaN doped with impurities to a concentration in the range of 5x10E14 to 5x10E17 per cm-3 (page 21).

Therefore it would obvious to one of ordinary skill in the art at the time the invention was made to adjust the modulation doped layer concentration as taught by

Parikh in the process of Nakamura in order to form a high quality film with improved crystallinity.

Furthermore parameters such as concentration in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the modulation doped layer concentration as claimed in the process of Nakamura in order to form a high quality film with improved crystallinity.

Regarding claim 2, Nakamura teaches substantially the entire claimed structure of claim 1 above including the forming step includes forming alternating sub-layers of doped nitride semiconductor and undoped nitride semiconductor (layer 4, [0054]) atop the at least portion of the another layer (3).

Regarding claim 4, Nakamura teaches substantially the entire claimed structure of claim 1 above except explicitly stating that diffusing dopants from the sub-layer of doped nitride semiconductor into the sub-layer of undoped nitride semiconductor to form the doped layer, the doped layer having a doping concentration that is substantially uniform.

It is conventional in the art to form doped regions by diffusing dopants from one layer to another. Furthermore parameters such as doping level in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to doped the doped layer as claimed in order to formed a layer with improved quality.

Regarding claims 5 and 6, Nakamura teaches substantially the entire claimed structure of claim 1 above including the modulation-doped layer includes a gallium nitride-based semiconductor and the modulation-doped layer included GaN ([0054]).

Regarding claim 7, Nakamura teaches substantially the entire claimed structure of claim 1 above including the modulation-doped layer is n-type (the modulation doped layer 4 has silicon as dopant hence n-type [0054]).

Regarding claim 8, Nakamura teaches substantially the entire claimed structure of claim 1 above including the modulation-doped layer has a doping concentration of at least $4E15cm^{-3}$ (the modulation doped layer has more than what is claimed, refer to [0054]).

Regarding claims 9-11, Nakamura teaches substantially the entire claimed structure of claim 1 above including the modulation-doped layer has a thickness of least 0.2 μm, or at most 10 μm (the modulation doped layer has a thickness of 1 μm, refer to [0054]) and the doped sub-layer is at least 0.005 μm ([0054]).

Regarding claims 12-13, Nakamura teaches substantially the entire claimed structure of claim 1 above except explicitly stating that the modulation-doped layer has a thickness of most 0.1 μm or the undoped sub-layer has a thickness of at least 0.005 μm.

Parameters such as thickness in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the thickness of the modulation doped layer as claimed in order to form a high quality film with improved crystallinity.

Regarding claim 14, Nakamura teaches substantially the entire claimed structure of claim 1 above including the undoped sub-layer of the modulation doped layer has a thickness of at most 0.1 μm (the undoped sub-layer has a thickness of 0.002 μm [0054]).

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, Parikh and in view of D' Evelyn et al., Pub. No. US 2002/0155634.

Nakamura teaches substantially the entire claimed process of claim 1 above except explicitly stating that the forming step is carried out by process selected from the group consisting of reactive sputtering, metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE) and atomic layer epitaxy.

D' Evelyn teaches forming a nitride-based layer by MOCVD (paragraph [0063]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the process of using MOCVD taught by D' Evelyn to form the modulation doped layer in the process of Nakamura in order to improve better coverage during deposition.

9. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, Parikh and in view of Lee et al., Pub. No. US 2001/0034116.

Regarding claim 15, Nakamura teaches substantially the entire claimed structure of claim 1 above except explicitly stating that forming a Schottky junction includes forming a metal contact layer atop the modulation doped layer.

It is conventional to form Schottky junction and is also taught by Lee (fig. 8) forming a Schottky contact/junction by forming a metal contact (44) in the process of forming a semiconductor device with a Schottky contact.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Schottky junction taught by Lee in the process of Nakamura in order to form a rectifying junction with an excellent electrical characteristics.

Regarding claim 16, Nakamura teaches substantially the entire claimed structure of claims 1 and 15 above except explicitly stating forming an ohmic contact on another portion of the another layer.

It is conventional to form an ohmic contact and is also taught by Lee (fig. 8) forming an ohmic contact by forming contact (45) in the process of forming a semiconductor device with an ohmic contact.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the ohmic contact taught by Lee in the process of Nakamura in order to form a contact with an excellent electrical characteristics.

10. Claims 17 and 19-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over D' Evelyn et al., Pub. No. US 2002/0155634 in view of Parikh.

Regarding claim 17, D' Evelyn teaches (fig. 4) method of forming a Schottky diode, the method comprising: forming a modulation doped layer (layers 302, 314) atop at least a portion another layer (316) by forming at least one sub-layer of doped nitride semiconductor (314) and at least one sub-layer undoped nitride semiconductor (302, layer 302 is insulating, therefore inherently undoped; layers 302 and 316 are based on $Ga_{1-x}Al_xN$) atop the at least portion of the another layer (316); forming a metallic contact layer (310) atop at least part of the modulation doped layer (302, 314) to form a Schottky junction therewith (Schottky contact is formed between 210 and 302); and forming at least one further metallic contact layer (312) on at least part of the another layer (310) in substantially ohmic contact therewith (ohmic contact is formed between 312 and 316).

D' Evelyn does not explicitly teach that a ratio of an on-resistance of the Schottky diode to a breakdown voltage of the Schottky diode is at most $2x10^{-5}\ \Omega\ .cm^2$ /v.

Parikh teaches the breakdown voltage fields of 2x10E6 V/cm for a GaN based device. By finding the ratio of the on-resistance to the breakdown on can get the ratio of an on-resistance of the Schottky diode to a breakdown voltage of the Schottky diode. Since the combined process teaches the same layers as the claimed invention, the ratio of the on-resistance to the breakdown voltage would closer the claimed invention.

Furthermore parameters such as ratio of on-resistance to breakdown voltage in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the ratio of on-resistance to the breakdown voltage as claimed in order to form a diode with better electrical characteristics.

Regarding claim 19, D' Evelyn teaches substantially the entire claimed process of claim 17 above including the step of forming the modulation doped layer is carried out by MOCVD (paragraph [0063]).

Regarding claims 20 and 21, D' Evelyn teaches substantially the entire claimed process of claim 17 above including a gallium nitride-based semiconductor and includes GaN (paragraph [0052]).

Regarding claim 22, D' Evelyn teaches substantially the entire claimed process of claim 17 above including the modulation-doped layer is n-type (fig. 4).

Regarding claims 23 and 24, D' Evelyn teaches substantially the entire claimed process of claim 17 above including the modulation doped has a thickness of at least 0.2 μm or at most 10 μm (layer 316 is in the range of 1-10 μm).

Regarding claim 25, D' Evelyn teaches substantially the entire claimed process of claim 17 above including the doped sub-layer of the modulation doped layer has a thickness of at least 0.005 μm (layer 316 is in the range of 1nm -10 μm).

Regarding claims 26-28, D' Evelyn teaches substantially the entire claimed process of claim 17 above except explicitly stating that the doped sub-layer modulation-

doped layer has a thickness of at most 0.1 μm, the undoped sub-layer has a thickness of at least 0.005 μm or at most 0.1 μm.

Parameters such as thickness in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the thickness of both the doped and undoped sub-layers of the modulation doped layer as claimed in order to form a high quality film with improved crystallinity.

Regarding claim 29, D' Evelyn teaches substantially the entire claimed process of claim 17 above including the first metal contact layer is nickel ([0053]).

Regarding claim 30, as best the examiner is able to ascertain the claimed process, D' Evelyn teaches substantially the entire claimed process of claim 17 above including the another layer comprises doped layer of nitride (316) semiconductor that is formed atop a substrate (306) prior to forming the modulation doped layer (302,314), the modulation-doped layer and the another doped layer (316) being of the same conductivity type (n-type).

D' Evelyn does not explicitly teach, the another doped layer being more highly doped than the modulation-doped layer.

Parameters such as concentration in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the modulation doped layer concentration and another doped layer as claimed in the process of D' Evelyn in order to form a high quality film with improved crystallinity.

Regarding claims 31-33, D' Evelyn teaches substantially the entire claimed process of claim 17 above including the another doped layer includes a gallium nitride-based (refer to [0052]) semiconductor, the another doped layer includes GaN ([0052]) and the another doped layer is n-type ([0052]).

Regarding claim 34, D' Evelyn teaches substantially the entire claimed process of claim 17 except explicitly stating that the another doped layer has a doping concentration of at least 4E18 cm^{-3}.

Parameters such as concentration in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the another doped layer concentration as claimed in the process of D' Evelyn in order to form a high quality film with improved crystallinity.

Regarding claim 35, D' Evelyn teaches substantially the entire claimed process of claim 17 above except explicitly stating said substrate is selected from the group consisting of sapphire, silicon carbide, doped silicon and undoped silicon.

However D' Evelyn teaches in paragraph ([0003]) refers to the use of several process that are used to produce hetero-epitaxial growth of gallium nitride based on sapphire or silicon carbide.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to form GaN based device on SiC as claimed in the process of fig. 4 in order to form a device that performs better in high temperature environment.

11. Claims 18 and 71-73 are rejected under 35 U.S.C. 103(a) as being unpatentable over D' Evelyn, Parikh in view of Nakamura.

Regarding claim 18, D' Evelyn teaches substantially the entire claimed process of claim 17 above except explicitly stating that step of forming the modulation doped layer includes forming alternating sub-layers of doped nitride semiconductor and undoped nitride semiconductor atop the at least portion of the another layer.

Nakamura teaches the advantage of forming alternating layers of doped and undoped sub-layers of nitride semiconductors (4) in the process of forming nitride based semiconductor device (fig. 1) with improved crystallinity.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the process of forming a super lattice of doped and undoped layers taught by Nakamura in the process of D' Evelyn in order to improve the crystallinity of the layers.

Regarding claim 71, D' Evelyn teaches (fig. 4) a method of forming a Schottky diode, the method comprising: forming a lower layer of n-type doped nitride

semiconductor (316) atop a substrate (306); forming an upper layer (314, 302) atop at least a portion of the lower layer of nitride semiconductor (316), the sub-layers being formed metal organic chemical vapor deposition (MOCVD, paragraph [0063]), forming a first metal contact layer (310) atop the upper layer of nitride semiconductor (302) such that a Schottky contact is formed (contact between 302 and 310); and forming a second metal contact layer (312) atop the lower layer of nitride semiconductor (316) such that an ohmic contact is formed (contact between 316 and 312).

D' Evelyn does not explicitly teach that forming the upper top layer by forming alternating sub-layers of n-type doped nitride semiconductor and undoped nitride semiconductor or the lower layer of nitride semiconductor being more highly doped than the upper layer of nitride semiconductor and a ratio of an on-resistance of said Schottky diode to a breakdown voltage of said Schottky diode is at most $2x10^{-5}$ Ω .cm^2 /v.

Nakamura teaches the advantage of forming alternating layers of doped and undoped sub-layers of nitride semiconductors (4) in the process of forming nitride based semiconductor device (fig. 1) with improved crystallinity.

Parikh teaches the breakdown voltage fields of 2x10E6 V/cm for a GaN based device. By finding the ratio of the on-resistance to the breakdown on can get the ratio of an on-resistance of the Schottky diode to a breakdown voltage of the Schottky diode. Since the combined process teaches the same layers as the claimed invention, the ratio of the on-resistance to the breakdown voltage would closer the claimed invention.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the process of forming a super lattice doped and

undoped layer taught by Nakamura in the process of D' Evelyn in order to improve the crystallinity of the layers.

Furthermore parameters such as concentration and ratio of on-resistance to breakdown voltage in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the upper layer doping layer concentration and the ratio of on-resistance to breakdown voltage as claimed in the process of D' Evelyn in order to form a high quality film with improved crystallinity.

Regarding claim 72, D' Evelyn teaches substantially the entire claimed process of claim 71 above including the at least one of the upper layer (302) of nitride semiconductor and the lower layer (314) of nitride semiconductor includes a gallium nitride-based semiconductor (paragraph [0052]).

Regarding claim 73, D' Evelyn teaches substantially the entire claimed process of claim 71 above including at least one of the upper layer (302) of nitride semiconductor and the lower layer (314) of nitride semiconductor includes GaN (paragraph [0052]).

12. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over D' Evelyn, Parikh in view of Sheu et al., US patent No. 6,712,478.

Regarding claim 36, D' Evelyn teaches substantially the entire claimed process of claim 17 above except explicitly stating that the ohmic metal contact layer is selected

from the group consisting of aluminum/titanium/platinum/gold (Al/Ti/Pt/Au) and titanium/aluminum/platinum/gold (Ti/Al/Pt/Au).

However Sheu teaches (fig.3) where the ohmic metal contact layer (162) is formed of Ti/Al/Pt/Au in the process of forming light emitting device.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the ohmic metal contact taught by Sheu in the process of D' Evelyn in order to reduce the contact resistance.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
December 7, 2005

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